

This listing of claims will replace all prior versions and listings of claims in the application:

1           2.. (Original) The computer implemented method of claim 1,  
2   wherein:  
3           said polynomial is a third degree polynomial of the form

5 where: y is the pixel output value to be computer; a is a first  
6 coefficient; b is a second coefficient; c is a third coefficient;  
7 and x is the pixel input value.

3. (Canceled)

1 4. (Original) The computer implemented method of claim 2,  
2 wherein:

3 said step of computing a pixel output value computes a first  
4 pixel output value and a second pixel output value by sequentially

5 (1) multiplying a first pixel input value by a first  
6 coefficient corresponding to said first pixel producing a  
7 first intermediate value,

8 (2) simultaneously multiplying a second pixel input value  
9 by a first coefficient corresponding to said second pixel  
10 producing a second intermediate value, and adding a second  
11 coefficient corresponding to said first pixel to said first  
12 intermediate value producing a third intermediate value,

13 (3) simultaneously multiplying said third intermediate  
14 value by said first pixel input value producing a fourth  
15 intermediate value, and adding a second coefficient  
16 corresponding to said second pixel to said second intermediate  
17 value producing a fifth intermediate value,

18 (4) simultaneously multiplying said fifth intermediate  
19 value by said second pixel input value producing a sixth  
20 intermediate value, and adding said third coefficient  
21 corresponding to said first pixel to said fourth intermediate  
22 value producing a seventh intermediate value,

23 (5) simultaneously multiplying said seventh intermediate  
24 value by said first pixel input value producing said first  
25 pixel output value, and adding said third coefficient  
26 corresponding to said second pixel to said sixth intermediate  
27 value producing an eighth intermediate value, and

28 (6) multiplying said eighth intermediate value by said  
29 second pixel input value producing said second pixel output  
30 value.

1        5. (Original) The computer implemented method of claim 4,  
2 wherein:  
3        said pixel input values are represented in a fixed point  
4 representation of 8 bits including zero integer bits and eight  
5 fractional bits;  
6        said first, second and third coefficients corresponding to  
7 each tone curve are represented in a fixed point representation of  
8 16 bits including four integer bits and twelve fractional bits;  
9        said step of adding said second coefficient corresponding to  
10 said first pixel to said first intermediate value producing a third  
11 intermediate value includes right shifting said first intermediate  
12 value 8 bits prior to addition;  
13        said step of adding said second coefficient corresponding to  
14 said second pixel to said second intermediate value producing a  
15 fifth intermediate value includes right shifting said second  
16 intermediate value by 8 bits prior to addition;  
17        said step of adding said third coefficient corresponding to  
18 said first pixel to said fourth intermediate value producing a  
19 seventh intermediate value includes right shifting said fourth  
20 intermediate value by 8 bits prior to addition; and  
21        said step of adding said third coefficient corresponding to  
22 said second pixel to said sixth intermediate value producing an  
23 eighth intermediate value includes right shifting said sixth  
24 intermediate value by 8 bits prior to addition.

1        6. (Original) A printer comprising:  
2        a transceiver adapted for bidirectional communication with a  
3 communications channel;  
4        a memory;  
5        a print engine adapted for placing color dots on a printed  
6 page according to received image data and control signals; and

7 a programmable data processor connected to said transceiver,  
8 said memory and said print engine, said programmable data processor  
9 programmed to:

10 receive print data corresponding to pages to be printed  
11 from the communications channel via said transceiver;

12 convert said print data into image data and control  
13 signals for supply to said print engine for printing a  
14 corresponding page, said conversion including approximating a  
15 gray scale tone with a more limited range print engine by

16 storing polynomial coefficients approximating each  
17 of a plurality of tone curves in a look-up table,

18 mapping each pixel of an image to a corresponding  
19 pixel of a screening matrix;

20 for each pixel of said image

21 recalling a corresponding set of polynomial  
22 coefficients approximating a tone curve associated  
23 with said pixel of said screening matrix mapped to  
24 said pixel, and

25 computing a pixel output value from a pixel  
26 input value of said pixel and said recalled  
27 polynomial coefficients.

1 7. (Original) The printer of claim 6, wherein:

2 said programmable data processor including a hardware  
3 multiplier and an arithmetic logic unit, said programmable data  
4 processor being further programmed to compute said pixel output  
5 value by

6 multiplying said pixel input value by said first  
7 coefficient in said hardware multiplier producing a first  
8 intermediate value,

9           adding said second coefficient to said first intermediate  
10 value in said arithmetic logic unit producing a second  
11 intermediate value,  
12           multiplying said second intermediate value by said pixel  
13 input value in said hardware multiplier producing a third  
14 intermediate value,  
15           adding said third coefficient to said third intermediate  
16 value in said arithmetic logic unit producing a fourth  
17 intermediate value, and  
18           multiplying said fourth intermediate value by said pixel  
19 input value in said hardware multiplier producing said pixel  
20 output value.

1       8. (Original) The printer of claim 6, wherein:  
2       said programmable data processor including a hardware  
3 multiplier and an arithmetic logic unit, said programmable data  
4 processor being further programmed to compute said pixel output  
5 value by  
6       (1) multiplying a first pixel input value by a first  
7 coefficient corresponding to said first pixel in said hardware  
8 multiplier producing a first intermediate value,  
9       (2) simultaneously multiplying a second pixel input value  
10 by a first coefficient corresponding to said second pixel in  
11 said hardware multiplier producing a second intermediate  
12 value, and adding a second coefficient corresponding to said  
13 first pixel to said first intermediate value in said  
14 arithmetic logic unit producing a third intermediate value,  
15       (3) simultaneously multiplying said third intermediate  
16 value by said first pixel input value in said hardware  
17 multiplier producing a fourth intermediate value, and adding a  
18 second coefficient corresponding to said second pixel to said

19 second intermediate value in said arithmetic logic unit  
20 producing a fifth intermediate value,

21 (4) simultaneously multiplying said fifth intermediate  
22 value by said second pixel input value in said hardware  
23 multiplier producing a sixth intermediate value, and adding  
24 said third coefficient corresponding to said first pixel to  
25 said fourth intermediate value in said arithmetic logic unit  
26 producing a seventh intermediate value,

27 (5) simultaneously multiplying said seventh intermediate  
28 value by said first pixel input value in said hardware  
29 multiplier producing said first pixel output value, and adding  
30 said third coefficient corresponding to said second pixel to  
31 said sixth intermediate value in said arithmetic logic unit  
32 producing an eighth intermediate value, and

33 (6) multiplying said eighth intermediate value by said  
34 second pixel input value in said hardware multiplier producing  
35 said second pixel output value.

1 9. (Original) The printer of claim 8, wherein:  
2 said programmable data processor further including a shifter  
3 at one input to said arithmetic logic unit, said programmable data  
4 processor being further programmed to compute said pixel output  
5 value by  
6 right shifting said first intermediate value 8 bits prior  
7 to addition;  
8 right shifting said second intermediate value by 8 bits  
9 prior to addition;  
10 right shifting said fourth intermediate value by 8 bits  
11 prior to addition; and  
12 right shifting said sixth intermediate value by 8 bits prior to  
13 addition.